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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/083,756	02/25/2002	Do-Hyung Kim	4591-227	2262

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EXAMINER	
HU, SHOUXIANG	
ART UNIT	PAPER NUMBER
2811	

SHORTENED STATUTORY PERIOD OF RESPONSE	MAIL DATE	DELIVERY MODE
3 MONTHS	02/08/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

If NO period for reply is specified above, the maximum statutory period will apply and will expire 6 MONTHS from the mailing date of this communication.

Office Action Summary	Application No.	Applicant(s)	
	10/083,756	KIM ET AL.	
	Examiner	Art Unit	
	Shouxiang Hu	2811	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *22 November 2006*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-15,17,18,20-22 and 24-26* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-15,17,18,20-22 and 24-26* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Allowable Subject Matter

1. The indicated allowability of claims 15, 17, 18, 20 and 21 is withdrawn in view of newly discovered reference(s) to be cited in the office action.

Claim Objections

2. Claims 15, 17, 18, 20, 21, 25 and 26 are objected to because of the following informalities and/or defects:

The term of "the liner material layer" recited in these claims should read as: --the conformal liner material layer--.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claims 1-15, 17-18, 20-22 and 24-26 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

4. Claims 1 and 12 each recite the subject matters of "forming an oxide layer", "growing a thermal oxide layer" and "forming a CVD oxide layer". But, they each fail to definitely define the relationship(s) among these three layers; and/or they each fail to

clarify whether the thermal oxide layer and the CVD oxide layer are definitely comprised in the recited "an oxide layer". Without proper clarification, such indefiniteness may leads to various patentably distinctive interpretations that are not all always covered by the instant disclosure. For example, the invention as defined in the claims may cover the method of forming an oxide layer in addition to the steps of forming the bi-layer including the thermal oxide layer and the CVD oxide layer, wherein the "an oxide layer" and the bi-layer may be separated layers but still meet all the conditions on their thicknesses in the manner same as the one defined in the claims.

5. In claims 1 and 12, the meaning of the phrase involving "the CVD oxide layer having a third thickness substantially equal to a difference between the first thickness and the second thickness directly on the thermal oxide layer in the same CVD apparatus" is not definitely clear, as they each fail to clarify which layer is definitely on the thermal oxide layer, and/or whether the term of "directly on" refers "formed directly on".

6. Claims 4-6 and 10 recite the terms of "growing a thermal oxide layer" and/or "forming a CVD oxide layer", but fail to clarify their respective relationships with the same terms already recited in claim 1.

7. Claims 15 and 22 each recite the terms of "a single crystalline silicon substrate" and "of single crystalline silicon substrate", but fail to clarify what is/are their relationship(s).

8. Claim 15 recites the terms of "forming a layer", "forming a nitride liner layer", "forming an oxide layer, "forming a thermal oxide layer" and "forming a CVD conformal

liner layer". But, it fails to definitely define the relationship(s) among these layers; and/or they each fail to clarify which of these recited layer(s) is/are definitely in included in which of these recited layer(s).

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

10. Claims 1-10 and 12-14, insofar as being in compliance with 35 U.S.C. 112, and as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakamura (US 2002/0121661) in view of Suzuki (6,228,166) and/or Maeda (US 6,231,673) and/or Gilmer (US 5,904,542).

Nakamura discloses a method for forming an oxide layer, including a thermal oxide layer (9a) and a CVD oxide layer (10a), having a first thickness as the combined thickness in an integrated circuit device, the method (Fig. 4; also see Paragraph [0085]) naturally comprising: growing the thermal oxide layer (9a) having a second thickness thinner than the first thickness on a surface of a semiconductor substrate; and, after growing the thermal oxide layer (9a) and directly on it, forming the CVD oxide layer (10a) naturally in a chemical vapor deposition (CVD) apparatus, the CVD oxide layer having a third thickness naturally substantially equal to a difference between the first thickness and the second thickness/

Although Nakamura does not expressly disclose that the thermal oxide can also be formed inside the same CVD apparatus, one of ordinary skill in the art would readily recognize that such thermal oxide layer can be desirably formed in the same CVD apparatus, so as to simplify the process and/or reduce the process cost and/or time, as readily evidenced in Suzuki (col. 10, lines 13-27), and/or Maeda (col. 15, lines 50-55), and/or Gilmer (col. 4, lines 1-10).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to develop the method of Nakamura with the thermal oxide layer being formed in the same CVD apparatus, per the teachings of Suzuki and/or Maeda and/or Gilmer, so that a method for making an oxide layer with simplified process and/or with reduced process cost and/or time would be obtained.

Regarding claims 2, 6, 7, 8, 10-13, it is noted that the thicknesses of the thermal oxide layer and the CVD oxide layer, the temperatures for the thermal oxidation and the CVD, and/or, the substrate-consumed thickness associated with the thermal oxide layer, are all art-recognized important result-oriented parameters subject to routine experimentation and optimization; and, that each of the thicknesses and temperatures are respectively well within the corresponding parameter ranges commonly recognized in the art. Thus, it would be well within the ordinary skill in the art to develop the method collectively taught above with the corresponding thicknesses and temperatures being respectively about the ones as recited in the claims, so as to form the oxide layer with optimized performance and/or process, since it has been held that "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the

optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Regarding claim 4, it is noted that it is well known in the art that the gate layer (11) in Nakamura, which is readable as an "another material layer", can be commonly formed of polysilicon through CVD inside a CVD apparatus, as readily evidenced in the prior art such as Schwabe (US 4,510,670; col. 3, lines 50-53). Accordingly, it would be well within the ordinary skill in the art to further form the gate layer with polysilicon in the same CVD apparatus in the method collectively taught above, so that the gate therein would be formed with a simplified process.

Regarding claims 5, 9, 10 and 14, it is noted that it is well known that O2 and/or N2O are commonly used in the art to form a thermal oxide layer; and that the N2O and/or SiH4 are commonly used in the art to form a CVD oxide layer.

Regarding claim 8, it is further noted that the method of Nakamura further comprises a step of forming a trench into the substrate.

11. Claims 11, 15, 17-18, 20-22 and 24-26, insofar as being in compliance with 35 U.S.C. 112, and as being best understood in view of the claim objections above, are rejected under 35 U.S.C. 103(a) as being unpatentable over Agahi (US 6,140,208) in view of Nakamura (US 2002/0121661) and/or Nakanishi (US 6,103,557), and further in view of Suzuki (6,228,166) and/or Maeda (US 6,231,673) Gilmer (US 5,904,542).

Agahi discloses a method of forming a layer for an integrated circuit device (Figs. 5 and 6), comprising: forming a trench in substrate (that is commonly a single crystalline silicon) by etching; forming an oxide layer of a double layer structure (23 and 20) having

a first thickness as its total thickness on a surface of the trench; forming a nitride liner layer (43) on the oxide layer, and forming an oxide trench isolation material layer (47), wherein forming the oxide layer comprises: forming a thermal oxide layer having a second thickness (such as 50-100 A) on the trench; forming a conformal liner material layer having a third thickness (such as 50-300A) that is naturally substantially equal to a difference between the first thickness and the second thickness; and, wherein the substrate can naturally be consumed by a thickness within the recited thickness range of 8.8 A to 44 A, during the formation of the thermal oxide layer, since the thermal oxide layer can have a thickness of about 50-100 A.

Although Agahi does not expressly disclose that the thermal oxide, the conformal oxide liner and the nitride layer can all be formed inside a same CVD apparatus, one of ordinary skill in the art would readily recognize that an oxide liner can be desirably formed with CVD method so as to achieve the desired liner conformity, as evidenced in Nakamura (see the CVD oxide layer 10a in Fig. 4); that an oxide layer and a nitride layer can both be formed through CVD in a same CVD apparatus so as to simplify the process, as evidenced in Nakanishi (col. 5, lines 60-67); and, that the thermal oxidation process and the CVD process can be desirably carried out inside a same CVD apparatus, so as to simplify the process and/or reduce the process cost and/or time, as readily evidenced in Suzuki (col. 10, lines 13-27) and/or Maeda (col. 15, lines 50-55) and/or Gilmer (col. 4, lines 1-10).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to develop the method of Agahi with the thermal oxide

layer, the conformal oxide liner layer and the nitride liner layer being formed in the same CVD apparatus, per the teachings of Nakamura and/or Nakanishi, and/or the teachings of Suzuki and/or Maeda and/or Gilmer, so that a method for making trench structure having liner layers therein with simplified process and/or with reduced process cost and/or time would be obtained.

Regarding claims 20 and 25, it is noted that the temperatures for the thermal oxidation and the CVD are both art-recognized important result-oriented parameters subject to routine experimentation and optimization; and, that each of the temperatures are respectively well within the corresponding parameter ranges commonly recognized in the art. Thus, it would be well within the ordinary skill in the art to develop the method collectively taught above with the corresponding temperatures being respectively about the ones as recited in the claims, so as to form the oxide layer with optimized performance and/or process; since it has been held that "[W]here the general conditions of a claim are disclosed in the prior art, it is not inventive to discover the optimum or workable ranges by routine experimentation." In re Aller, 220 F.2d 454, 456, 105 USPQ 233, 235 (CCPA 1955).

Regarding claims 20 and 25, it is further noted that it is well-known that O2 and/or N2O are commonly used in the art to form a thermal oxide layer; and the N2O and/or SiH4 are commonly used in the art to form a CVD oxide layer.

Regarding claims 21-22 and 24-26, it is noted that it is well known in the art that the trench isolation material layer can be commonly formed through CVD. And, it would be well within the ordinary skill in the art to further form the trench isolation material

layer in the same CVD apparatus in the method collectively taught above, so as to further simplify the process and/or further reduce the process cost and/or time.

Response to Arguments

12. Applicant's arguments with respect to the claims rejected above have been considered but are moot in view of the new ground(s) of rejection.

Conclusion

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Reference E is cited as being related to a method of forming CVD gate layer.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Shouxiang Hu whose telephone number is 571-272-1654. The examiner can normally be reached on Monday through Friday, 8:30 AM to 5:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Richard T. Elms can be reached on 571-272-1869. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR.

Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

SH
February 3, 2007

SHOUXIANG HU
PRIMARY EXAMINER